Claim Amendments

Please amend claims 1, 6, 11, and 16 as follows:

Claims as Amended

What is claimed is:

1. (currently amended) A CMOS semiconductor product comprising:
a semiconductor substrate;

a first doped well of the first polarity and a laterally separated second doped well of a second polarity opposite the first polarity, both formed into the semiconductor substrate;

a third doped well of the second polarity laterally and vertically surrounding the first doped well of the first polarity; and

a metal oxide semiconductor transistor of the second polarity formed ~~within and~~ upon the first doped well and a metal oxide semiconductor transistor of the first polarity formed ~~within and~~ upon the second doped well.

2. (original) The CMOS semiconductor product of claim 1 further comprising a fourth doped well of the second polarity laterally adjoining but not vertically beneath the first doped well of the

first polarity.

3. (original) The CMOS semiconductor product of claim 1 wherein the third doped well is formed to a distance of from about 1000 to about 10000 angstroms beneath the first doped well.

4. (original) The CMOS semiconductor product of claim 2 wherein the second doped well is separated from the fourth doped well by a separation distance of less than about 15 microns.

5. (original) The CMOS semiconductor product of claim 1 wherein a guard ring is not employed surrounding either metal oxide semiconductor transistor.

6. (currently amended) A CMOS semiconductor product comprising:

a p semiconductor substrate;

a p doped well and a laterally separated first n doped well, both formed into the semiconductor substrate;

a second n doped well laterally and vertically surrounding the p doped well; and

a p metal oxide semiconductor transistor ~~within and~~ upon the first n doped well and a p metal oxide semiconductor transistor formed ~~within and~~ upon the first n doped well.

7. (original) The CMOS semiconductor product of claim 6 further comprising a third n doped well laterally adjoining but not vertically beneath the p doped well.

8. (original) The CMOS semiconductor product of claim 6 wherein the second n doped well is formed to a distance of from about 1000 to about 10000 angstroms beneath the p doped well.

9. (original) The CMOS semiconductor product of claim 7 wherein the first n doped well is separated from the third n doped well by a separation distance of less than about 15 microns.

10. (original) The CMOS semiconductor product of claim 6 wherein a guard ring is not employed surrounding either metal oxide semiconductor transistor.

11. (currently amended) A method for operating a CMOS semiconductor product comprising:

providing a CMOS semiconductor product comprising:

a semiconductor substrate;

a first doped well of the first polarity and a laterally separated second doped well of a second polarity opposite the first polarity, both formed into the semiconductor substrate;

a third doped well of the second polarity laterally and vertically surrounding the first doped well of the first polarity; and

a metal oxide semiconductor transistor of the second polarity formed ~~within and~~ upon the first doped well and a metal

oxide semiconductor transistor of the first polarity formed ~~within and~~ upon the second doped well; and

electrically energizing each of the metal oxide semiconductor transistors.

12. (original) The method of claim 11 wherein the CMOS semiconductor product further comprises a fourth doped well of the second polarity laterally adjoining but not vertically beneath the first doped well of the first polarity.

13. (original) The method of claim 11 wherein the third doped well is formed to a distance of from about 1000 to about 10000 angstroms beneath the first doped well.

14. (original) The method of claim 11 wherein the second doped well and the third doped well are held at the same voltage when electrically energizing the metal oxide semiconductor transistors.

15. (original) The method of claim 11 wherein a guard ring is not employed surrounding either metal oxide semiconductor transistor.

16. (currently amended) A method of operating a CMOS semiconductor product comprising:

providing a CMOS semiconductor product comprising:

a p semiconductor substrate;

a p doped well and a laterally separated first n doped well, both formed into the semiconductor substrate;

a second n doped well laterally and vertically surrounding the p doped well; and

a p metal oxide semiconductor transistor ~~within and~~ upon the first n doped well and a p metal oxide semiconductor transistor formed ~~within and~~ upon the first n doped well; and

electrically energizing each of the metal oxide semiconductor transistors.

17. (original) The method of claim 16 wherein the CMOS semiconductor product further comprises a third n doped well laterally adjoining but not vertically beneath the p doped well.

18. (original) The method of claim 16 wherein the second n doped well is formed to a distance of from about 1000 to about 10000 angstroms beneath the p doped well.

19. (original) The method of claim 16 wherein the first n doped well and the second n doped well are held at the same voltage when electrically energizing the metal oxide semiconductor transistors.

20. (original) The method of claim 16 wherein a guard ring is not employed surrounding either metal oxide semiconductor transistor.